Application Note 350
Provision Your DS2152 or DS2154 Hardware Design for the Next Generation Devices

The next generation of the DS2152/54 will be 3.3V and 5V pin compatible T1 and E1 chip sets with a new pin-out. Each of the T1 and E1 Single Chip Transceivers will be able, however, to drop into existing DS2152/54 sockets with no hardware or software changes (not using the new features). Be sure to write 00hex to existing but unused register locations. Unused register locations may be used for new features. Table 1 lists each of the DS2152/54 and DS21352/354/552/554 SCTs and the associated features.

DALLAS SEMICONDUCTOR 100–PIN LQFP SINGLE CHIP TRANSCEIVERS
Table 1

	DS2152L/ LN	DS21352L/ LN	DS21552L/ LN	DS2154L/ LN	DS21354L/ LN	DS21554L/ LN
T1	X	X	X			
E1				X	X	X
3.3V		X			X	
5V	X		X	X		X
JTAG		X	X		X	X
Interleaved PCM Bus		X	X		X	X
HDLC Controller	X[1]	X	X		X	X
TCMC		X	X		X	X

NOTE:
1. The DS2152 has an HDLC controller dedicated to FDL applications.

JTAG, IEEE 1149.1 BOUNDARY SCAN ARCHITECTURE
The new DS21352/354/552/554 SCTs will incorporate JTAG's Boundary Scan Architecture (IEEE 1149.1). The Framer ModeSelect (FMS) pin has an internal 10k pull up resistor which places the new SCTs in the DS2152/54 legacy mode. All JTAG pins can be left unconnected in the legacy mode. To use the JTAG features, a hardware change will be required to incorporate the 5 JTAG pins and the FMS pin will need to be tied LOW. The FMS and JTRST pins will affect the TESTZ pin (all four DS21x5y) and the TEST1 and TEST0 bits in the TCR2 register (both DS21x52). See Table 3 for JTRST and FMS conditions. Table 4 lists the new pin descriptions for the 3.3V I/O on the DS215y and the new pin descriptions for the new features on the DS21352/354/552/554 SCTs. Table 1 summarizes all of the SCTs in the 100 pin LQFP packages.

JTRST AND FMS CONDITIONS Table 3

JTRST	FMS	RESULT
X	1	TESTZ pin, TEST1 bit and TEST0 bits in TCR2 of DS21x52 enabled.
0	0	TEST1 bit and TEST0 bits in TCR2 of DS21x52 enabled.
1	0	0 TESTZ disabled, TEST1 and TEST0 bits in TCR2 of DS21x52 disabled.

NEW PIN DEFINITIONS FOR DS2152/54 AND DS21352/354/552/554 SCTs (DS2152/54 ONLY APPLY TO PINS 61 AND 83) Table 4

PIN	PREVIOUS SYMBOL	NEW SYMBOL	TYPE	DESCRIPTION
76	NC	FMS	I	**Framer Mode Select [FMS].** Selects the DS2152/54 mode when HIGH or the DS21x52/x54 mode when LOW. If High, the JTRST is internally pulled LOW. If LOW, JTRST has normal JTAG functionality. This pin has a 10k pull up resistor.
5	NC	JTRST	I	**IEEE 1149.1 Test Reset [JTRST].** This signal is used to asynchronously reset the test access port controller. At power up, JTRST must be toggled from LOW to HIGH. This action will set the device into the DEVICE ID mode allowing normal device operation. This pin has a 10k pull up resistor. When FMS=1, this pin is tied LOW internally. Tie JTRST LOW if JTAG is not used and the framer is in DS21x5y mode (FMS LOW).
2	NC	JTMS	I	**IEEE 1149.1 Test Mode Select [JTMS].** This pin is sampled on the rising edge of JTCLK and is used to place the test access port into the various defined IEEE 1149.1 states. This pin has a 10k pull up resistor.
4	NC	JTCLK	I	**IEEE 1149.1 Test Clock Signal [JTCLK].** This signal is used to shift data into JTDI on the rising edge and out of JTDO on the falling edge.
7	NC	JTDI	I	**IEEE 1149.1 [JTDO].** Test instructions and data are clocked into this pin on the rising edge of JTCLK. This pin has a 10k pull up resistor.
10	NC	JTDO	O	**IEEE 1149.1 [JTDO].** Test instructions and data are clocked out of this pin on the falling edge of JTCLK. If not used, this pin should be left unconnected.
36	NC	CI	I	**Carry In [CI]. Input.** A rising edge on this pin causes RSER and RSIG to come out of HIGH Z state and TSER and TSIG to start sampling on the next rising edge of RSYSCLK/TSYSCLK beginning an I/O sequence of 8 or 256 bits of data.
54	NC	CO	O	**Carry Out [CO].** An output which is set HIGH when the last bit of the 8 or 256 IBO output sequence has occurred on RSER and RSIG.

INTERLEAVED PCM BUS OPERATION (IBO)

The new DS21352/354/552/554 SCTs have a feature which will allow multiple SCTs to share a PCM bus for data or signaling. This is possible by internally gating the RSYSCLK and TSYSCLK inputs on the SCTs. When this feature is enabled 2 or 4 SCTs can share a 4.096 MHz or 8.192 MHz bus respectively. There are 4 register bits and two hardware pins which control the Interleaved Bus Operation (IBO). Using the IBO, the user must first set the IBOEN bit to a logic 1. Then select the byte or frame interleave mode via the INTSEL bit. MSEL1 and MSEL2 together determine both the slave or master mode for that specific SCT and how many SCTs are being multiplexed together. Two devices will require a 4.096 MHz clock to be applied to RSYSCLKs and TSYSCLKs while four devices will require an 8.192 MHz clock.

The elastic stores need to be enabled and set in the 2.048 MHz mode. Figure 1 shows the appropriate hardware connections.

The master SCT will not use the CI pin but will use the RSYNC/TSSYNC pins instead. The CI pin for the master SCT should be tied LOW. Each frame or multiframe SYNC/TSSYNC input signal will reset the IBO counters for each SCT and will enable the I/O of the master SCT to move 8 or 256 bits depending on byte or frame interleaving. On the 8^{th} or 256^{th} bit, the master CO pin will go HIGH. This signal can be used for the next SCT's CI pin. If at any time there is a new frame or multiframe RSYNC/TSSYNC input signal asynchronous to the existing frame or multiframe boundary, the IBO counters will be reset on the master SCT and each of the slaves. When an SCT is not actively outputting data, the RSER and RSIG pins will be in HIGH Z state. See Figure 2 for timing constraints and Table 7 for setup and delay times for CI and CO.

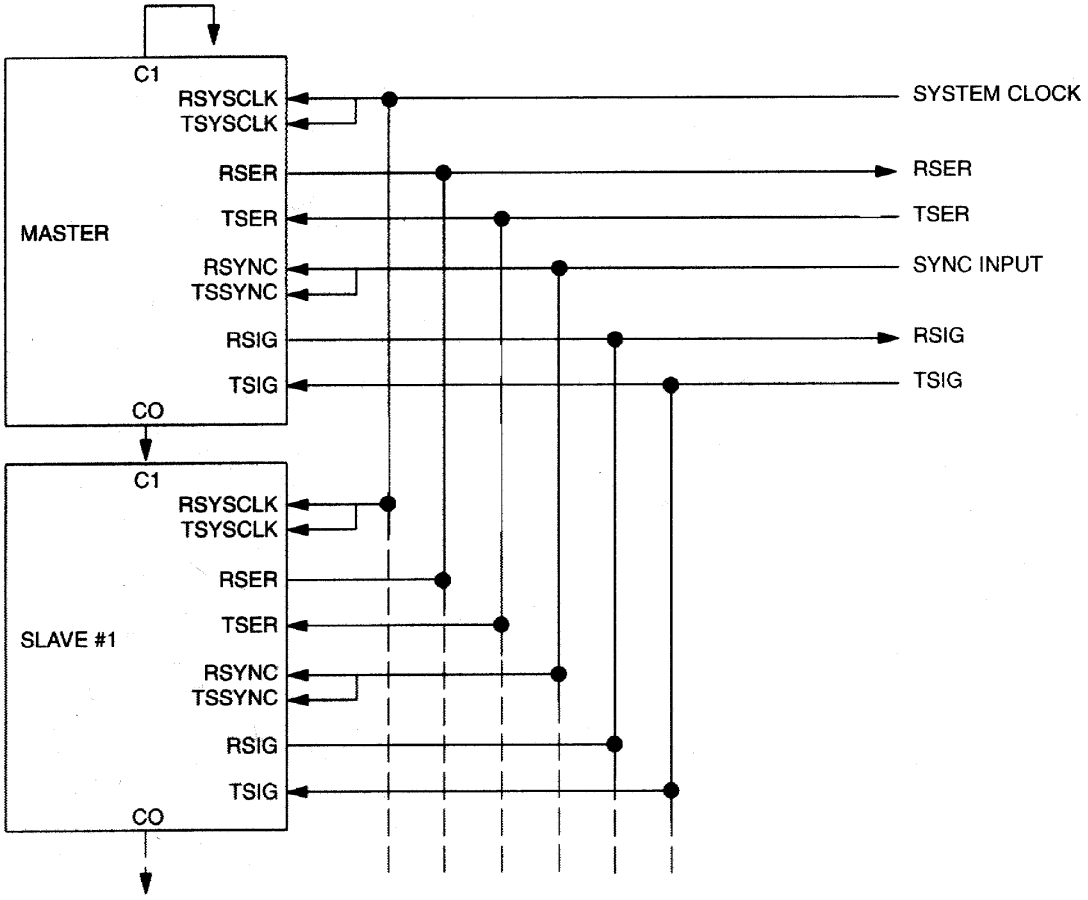
REGISTER BITS FOR IBO OPERATION Table 5

REGISTER BIT	DESCRIPTION	LOGIC '0'	LOGIC '1'
IBOEN	Interleaved Bus Operation Enable	IBO disabled	IBO disabled IBO enabled. In this mode, TSYSCLK and RSYSCLK must be connected together and elastic stores must be enabled in the 2.048 MHz mode.
INTEL	Interleave Select	Byte interleave	Frame interleave.
MSEL1	Master Select bit 1	See Table 6.	See Table 6.
MSEL2	Master Select bit 2	See Table 6.	See Table 6.

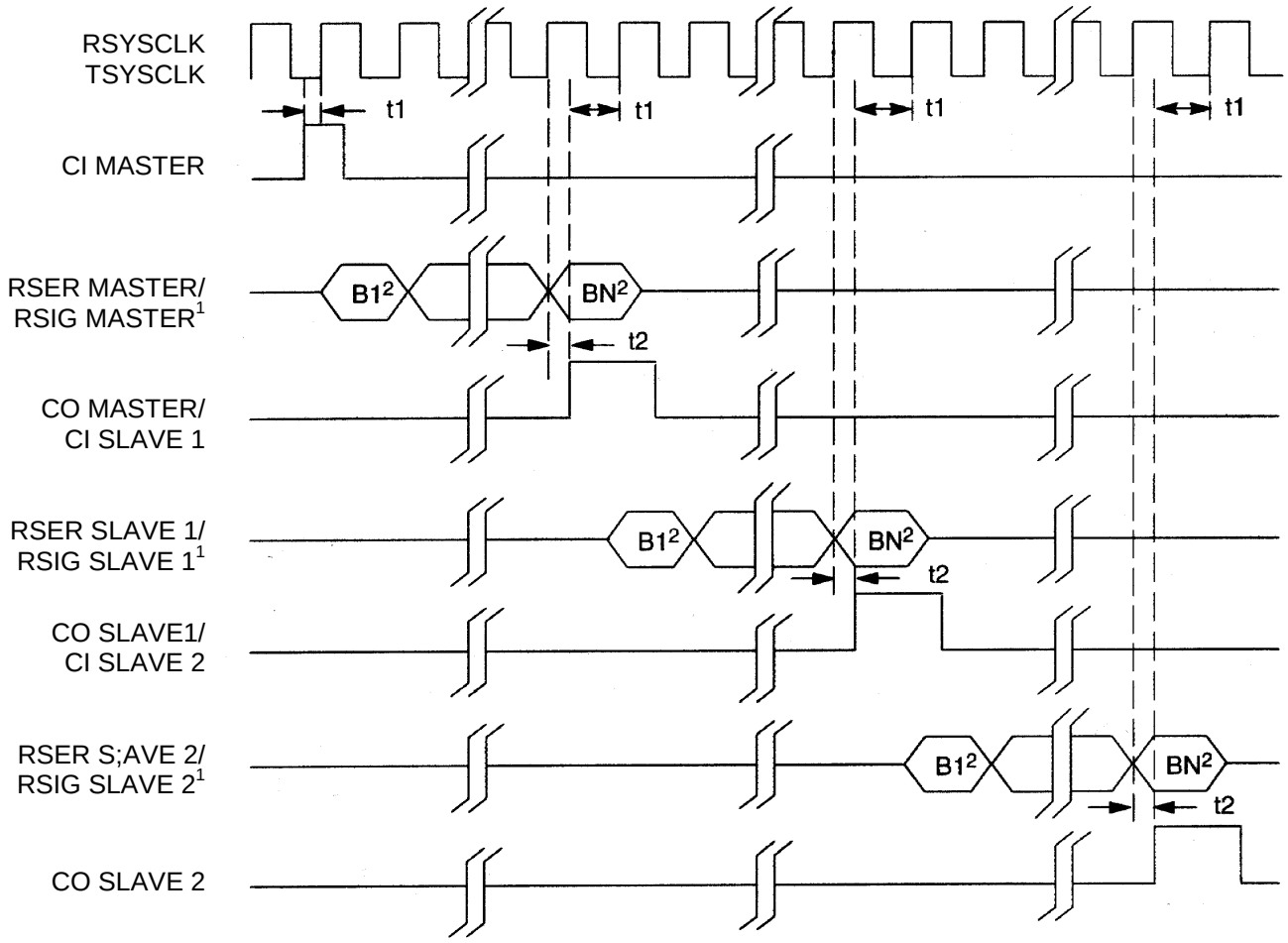
MSEL1 AND MSEL2 BIT FUNCTIONS Table 6

MSEL1	MSWL2	FUNCTION
0	0	SLAVE DEVICE
1	0	MASTER DEVICE WITH 1 SLAVE DEVICE (4.096 MHz CLOCK)
0	1	MASTER DEVICE WITH 3 SLAVE DEVICE (8.192 MHz CLOCK)

HARDWARE CONNECTIONS FOR IBO Figure 1



IBO TIMING Figure 2



NOTE1:

RSIG ONLY OUTPUTS DATA DURING THE LAST FOUR CLOCKS OF EACH TIME SLOT. REFER TO DATA SHEET.

NOTE 2:

B1 IS MSB. Bn IS LSB. n=8 FOR BYTE INTERLEAVED. n=256 FOR FRAME INTERLEAVED.

AC CHARACTERISTICS FOR IBO OPERATION Table 7

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Setup time for CI	t1	20			ns
Delay time after a rising edge on SYSCLK/ TSYSCLK. CO will stay HIGH for a full RSYSCLK/TSYSCLK period.	t2			50	ns

HDLC CONTROLLER

The DS21352/354/552/554 SCTs will contain an enhanced HDLC controller based on the existing HDLC controller in the DS2152. Each controller will have the following features:

- 64 byte buffers for the TX and RX
- Select any timeslot or multiple timeslots (even non contiguous timeslots) to be passed through the HDLC controller
- Select any bits within a single DS0 or the same bits within multiple DS0s

The HDLC controller in the DS21x52 SCTs will be completely backward compatible with the existing HDLC controller in the DS2152. The Bit Oriented Code (BOC) controller in the DS2152 will also be in the DS21x52 devices. This function is only necessary for Facility Data Link applications in the Extended Superframe Format (ESF) and is therefore omitted from the DS21x54 devices.

TRANSMIT CLOCK MUX CONTROL

The DS2152 and DS2154 have a Loss of Transmit Clock Mux Control (LOTCMC) bit in the TCR1 and CCR2 control registers respectively. Enabling these bits allows TCLK to be connected to RCLKO internally if no transition occurs at TCLK. The new TCMC bit enables TCLK to be connected to RCLKO internally regardless of the condition on the TCLK pin.